Open-Source Radio Microcontroller for Fabrication

ECPE Senior Design May 2025, Team 27

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Faculty Advisor and Client: Dr. Henry Duwe

Team Website: https://sdmay25-27.sd.ece.iastate.edu/

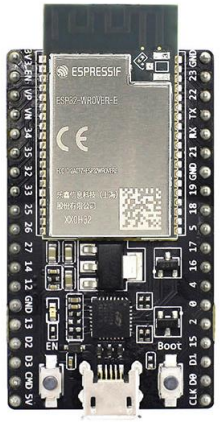
References to Design Document on slides as DD <page number>

IOWA STATE UNIVERSITY

Problem Statement

The lack of open-source radio microcontroller designs makes learning about radio design for fabrication difficult for students and hobbyists.

Closed Source Radio Microcontrollers



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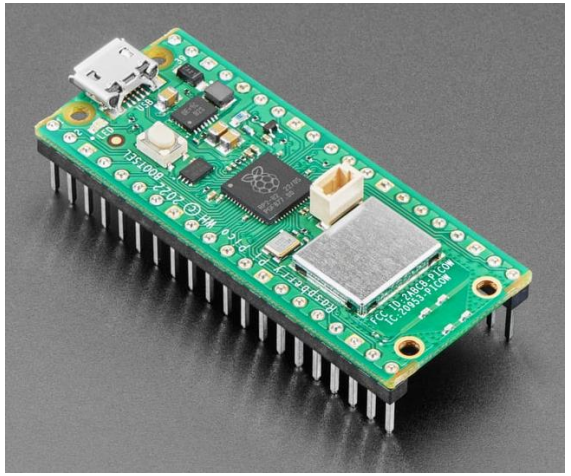

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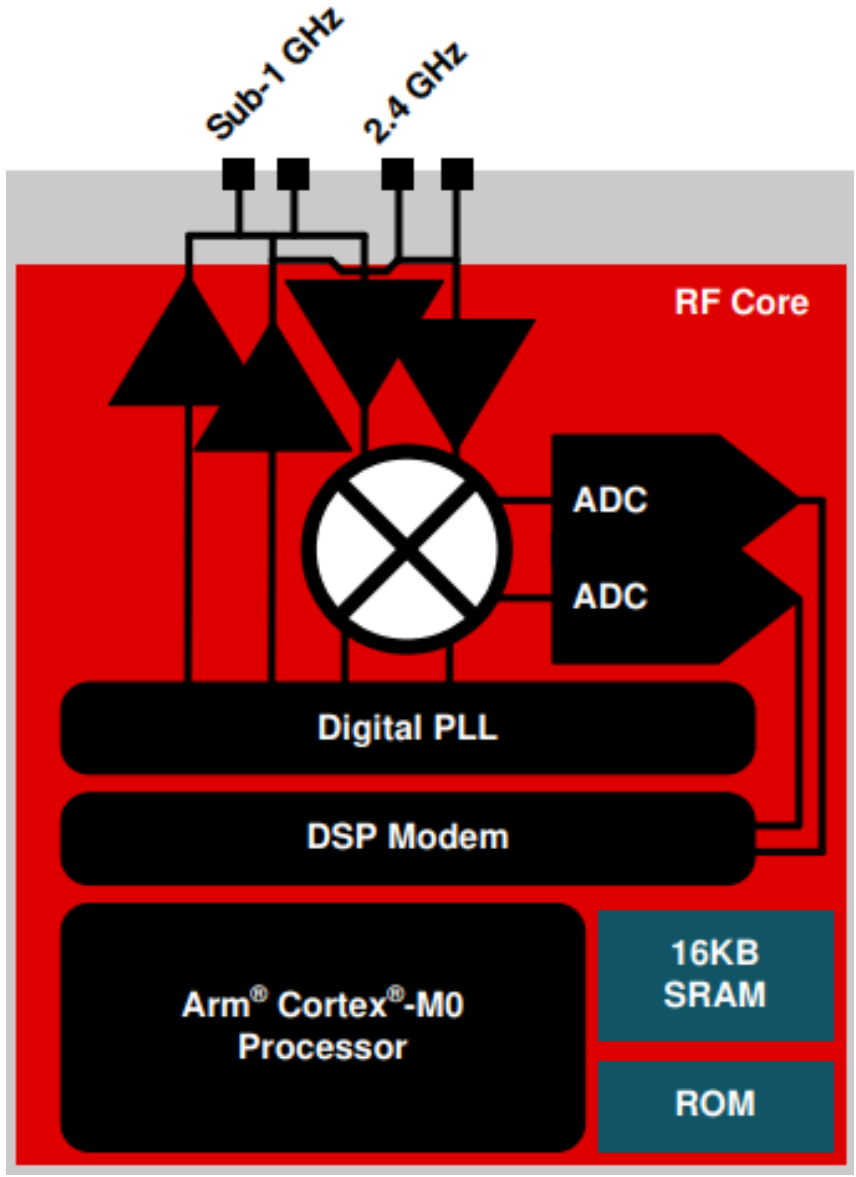
DD 13

Market Research – Texas Instruments CC1352

- Example of RF core architecture
- Provides a variety of wireless communication protocols
  - Thread
  - Zigbee
  - Bluetooth
- Multiple transmission frequencies
  - Ultra High (Sub GHz)
  - Super High (2.4 GHz)



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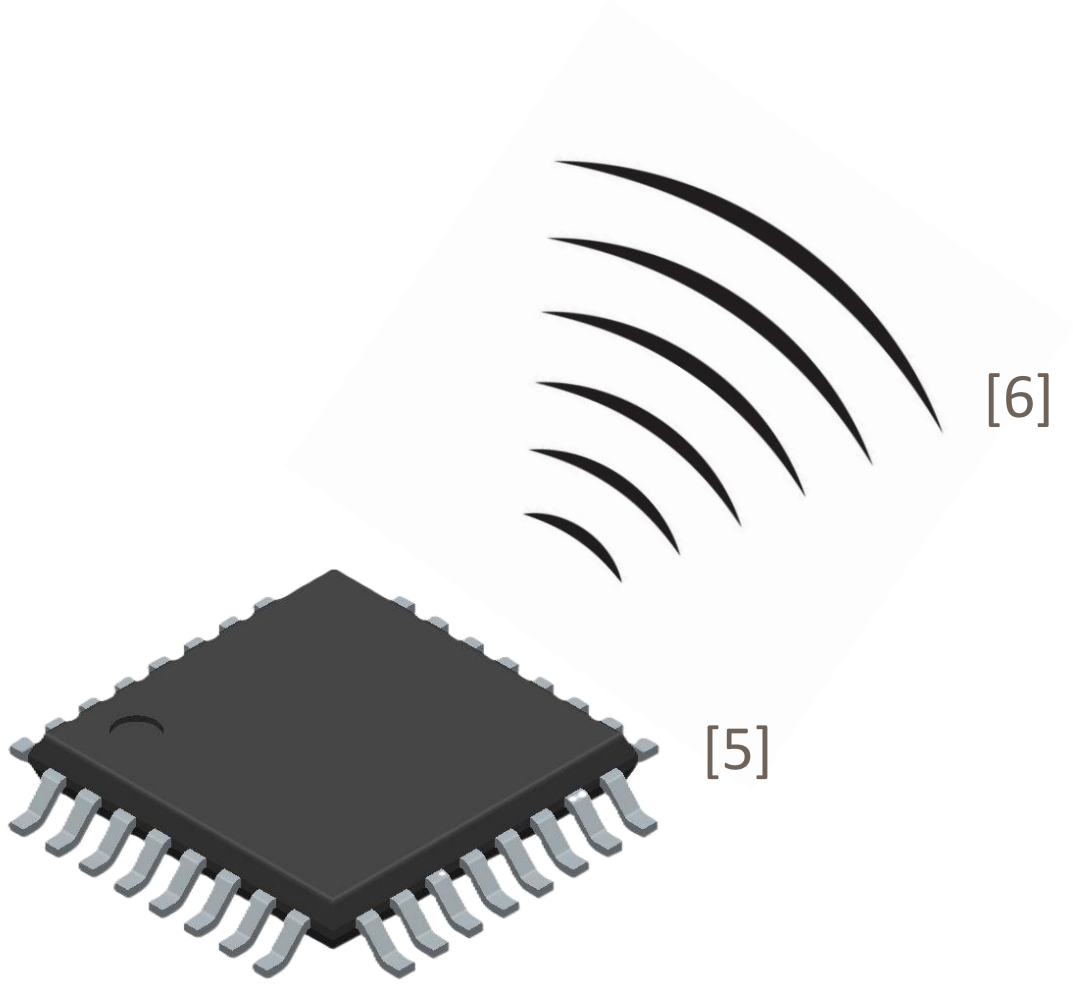
Requirements

- MCU shall contain a radio subsystem
- MCU shall implement an open standard wireless protocol stack
- MCU shall contain two independent RISC-V cores to execute user programs
- All the artifacts produced throughout the design of the MCU shall be open source.
- Thorough documentation usable by students with only basic knowledge of circuits and digital logic.
- DD 14



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Technologies Used

- Skywater 130 nm process
  - Provided by Efabless
  - Constraint from client
- Caravel Harness
  - Proven wrapper for project
- Openlane
  - Open-source tool for hardening digital designs
- GNU Compiler Collection (GCC)
  - Compile C programs for RISC-V processors
- Icarus Verilog
  - Simulate digital components to verify functionality
- NGSPICE
  - Simulate analog components to verify functionality

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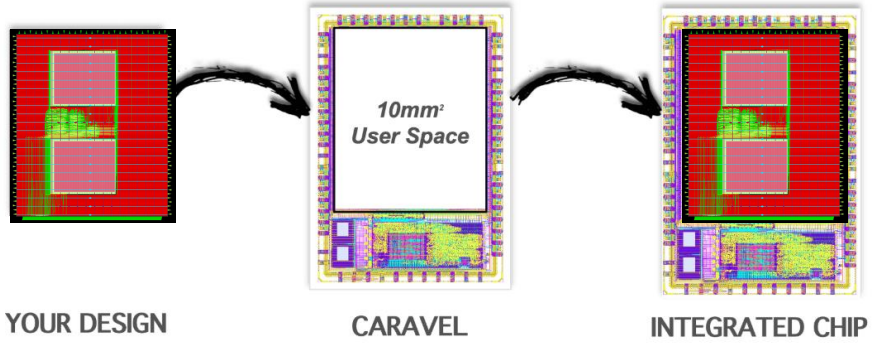

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Choosing a Wireless Communication Standard

- What wireless communication standard will we implement?
- Two major contenders:
  - Bluetooth and Zigbee
- Bluetooth operates at 2.4 GHz while ZigBee operates at ~915 MHz
- ZigBee is an open standard while Bluetooth is not.
- DD 40

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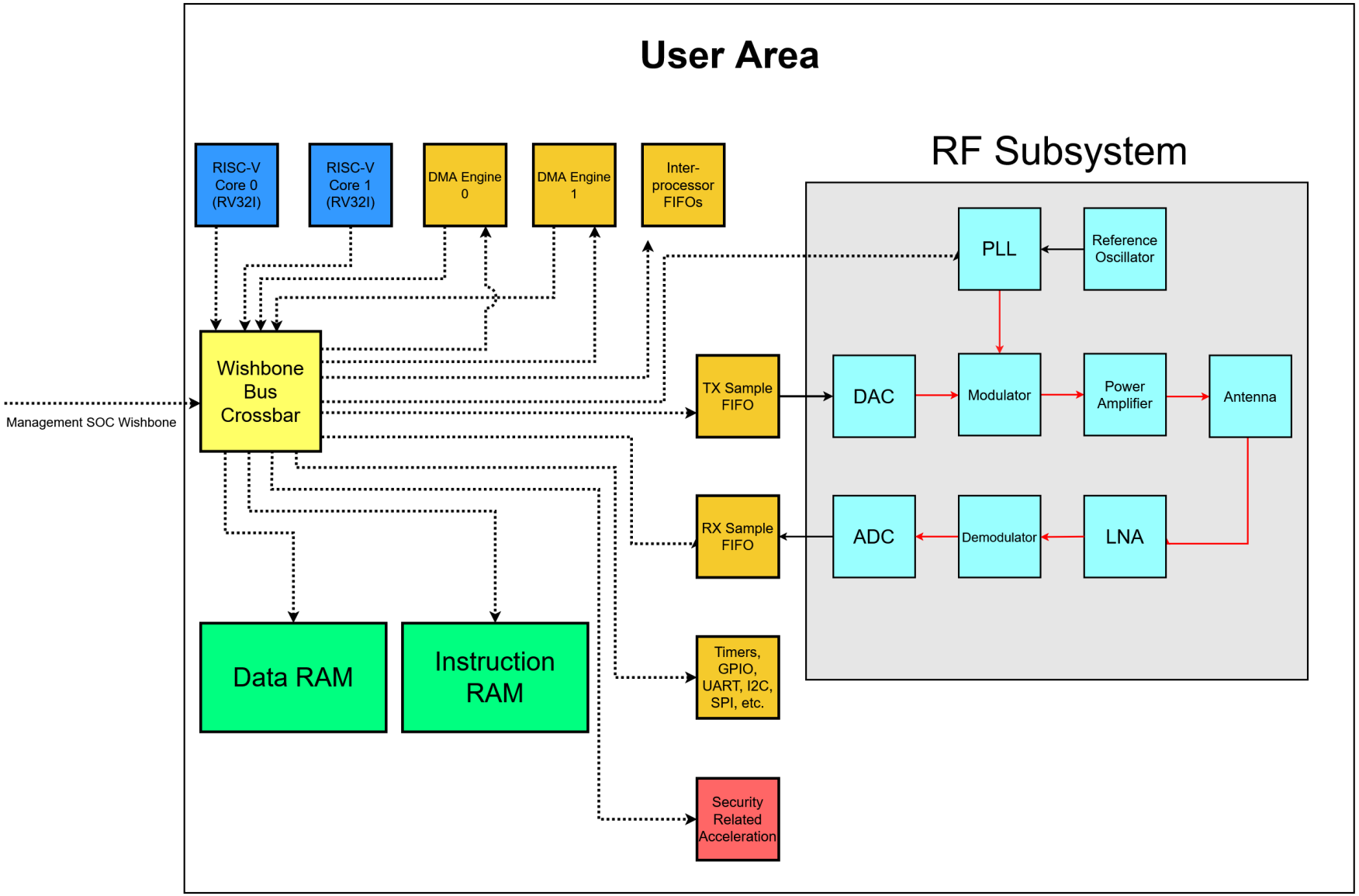
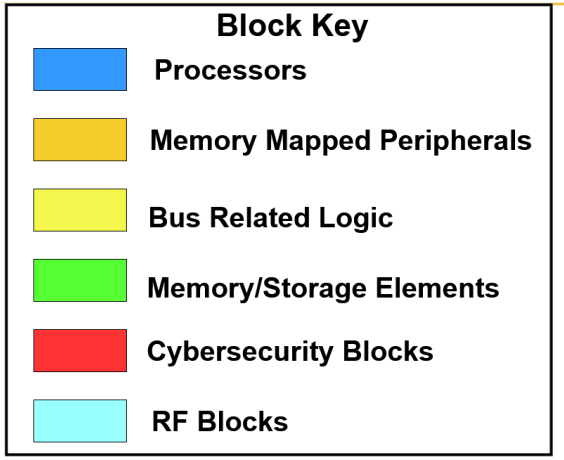
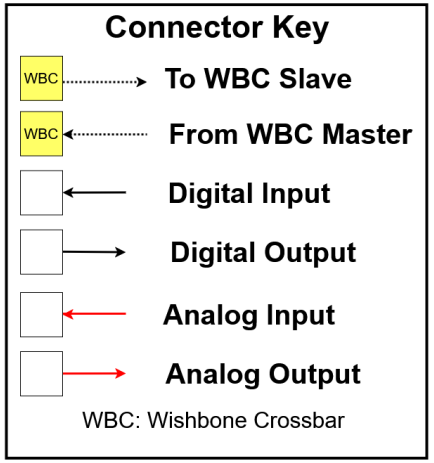
Detailed Design





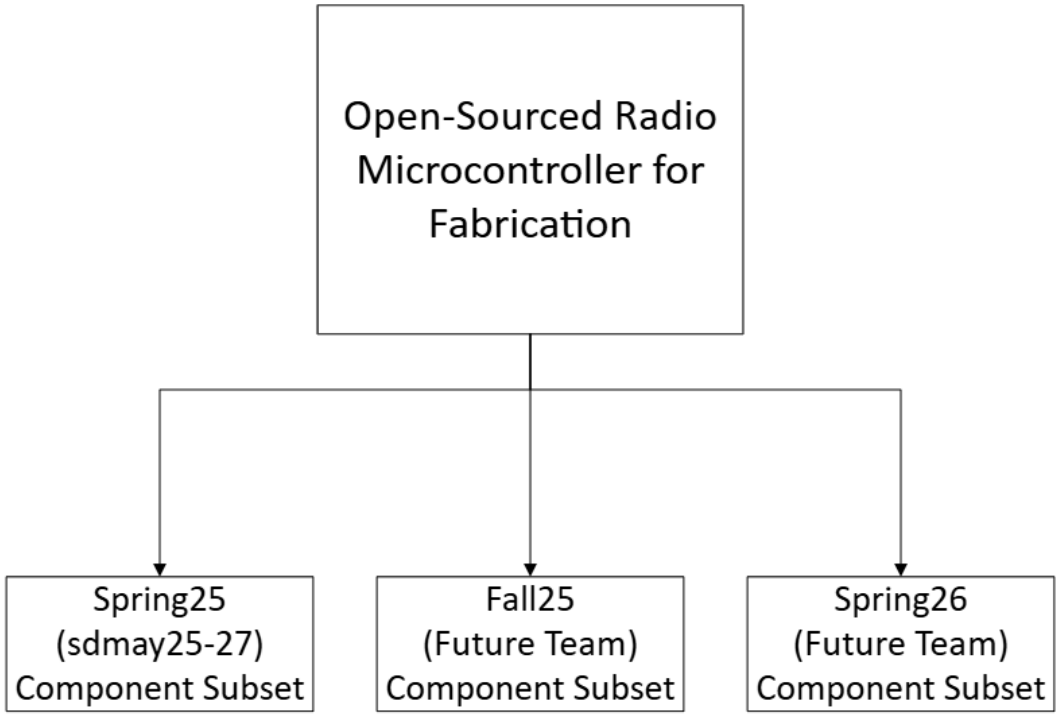


DD 57

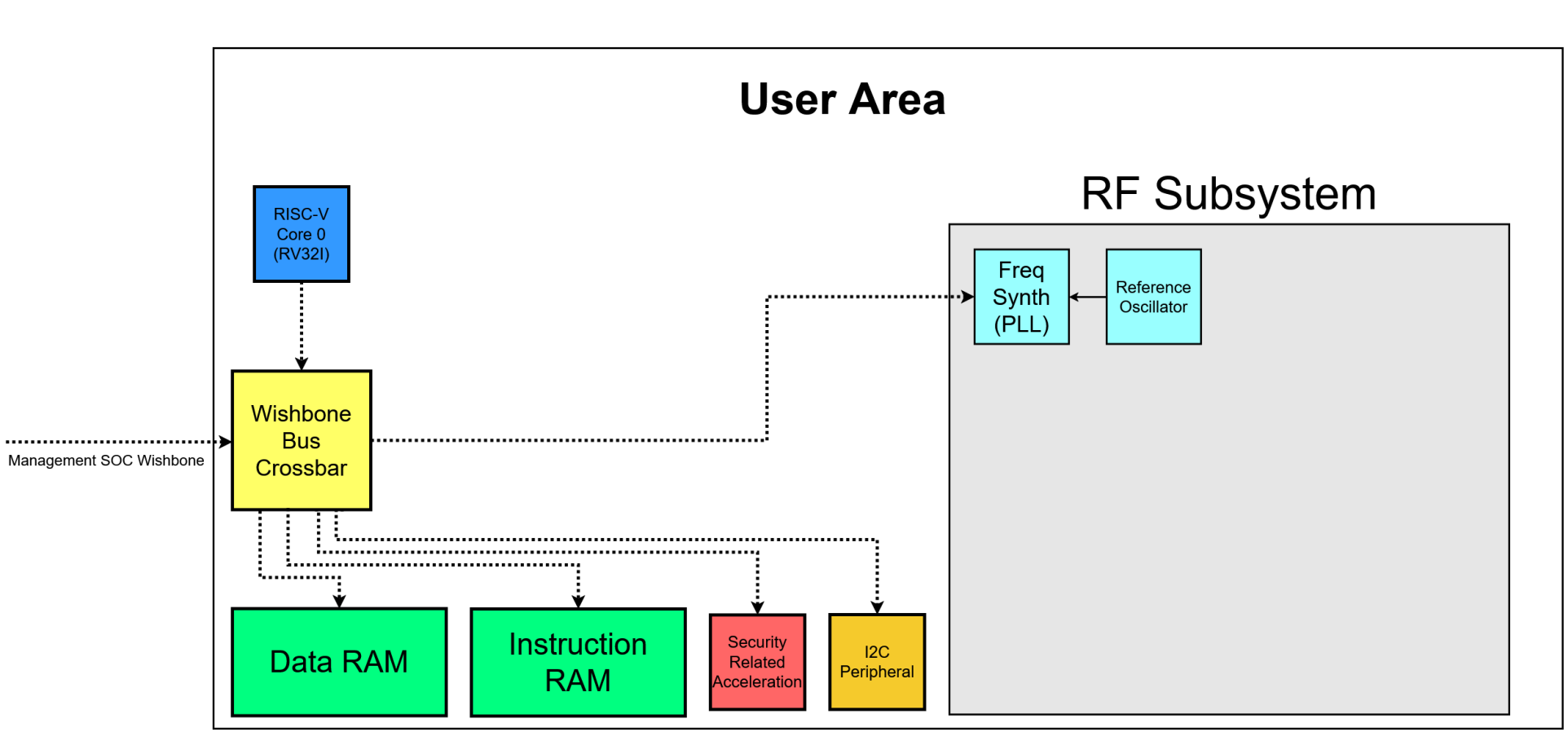
Potential Risks and Mitigation

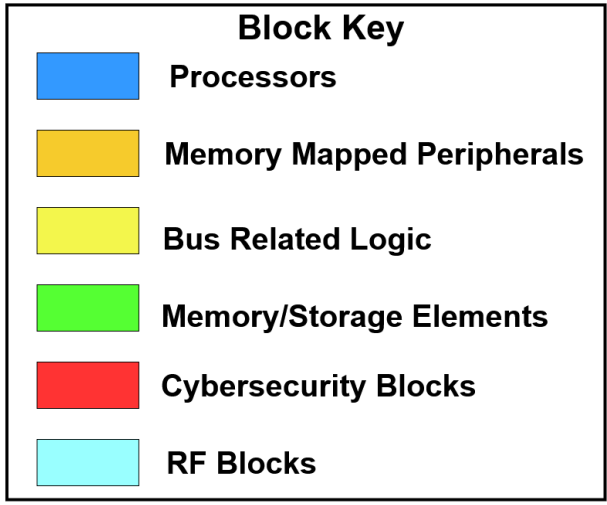
Unknown open-source tools

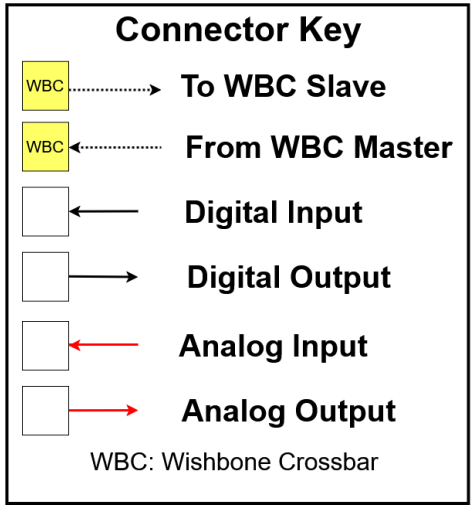
- Risks
  - Open-source tooling is different than tools team members have experience with
  - Less support and documentation
- Mitigation
  - We have created a design outline for the complete project
  - We have chosen a subset of components to implement
  - Weekly meetings with client/advisor to update on status and keep scope reasonable
- DD 25



May 2025 Component Subset



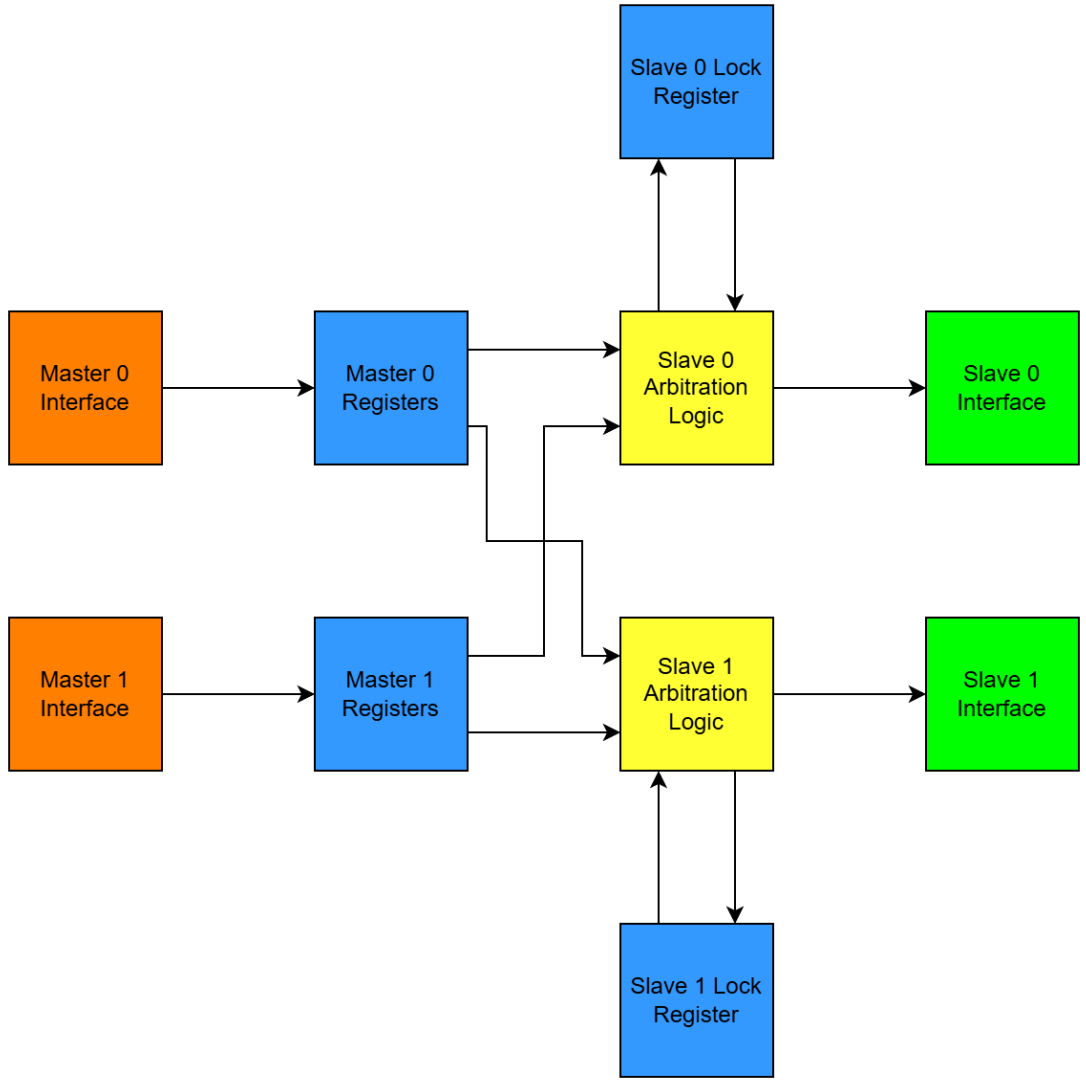




DD 57

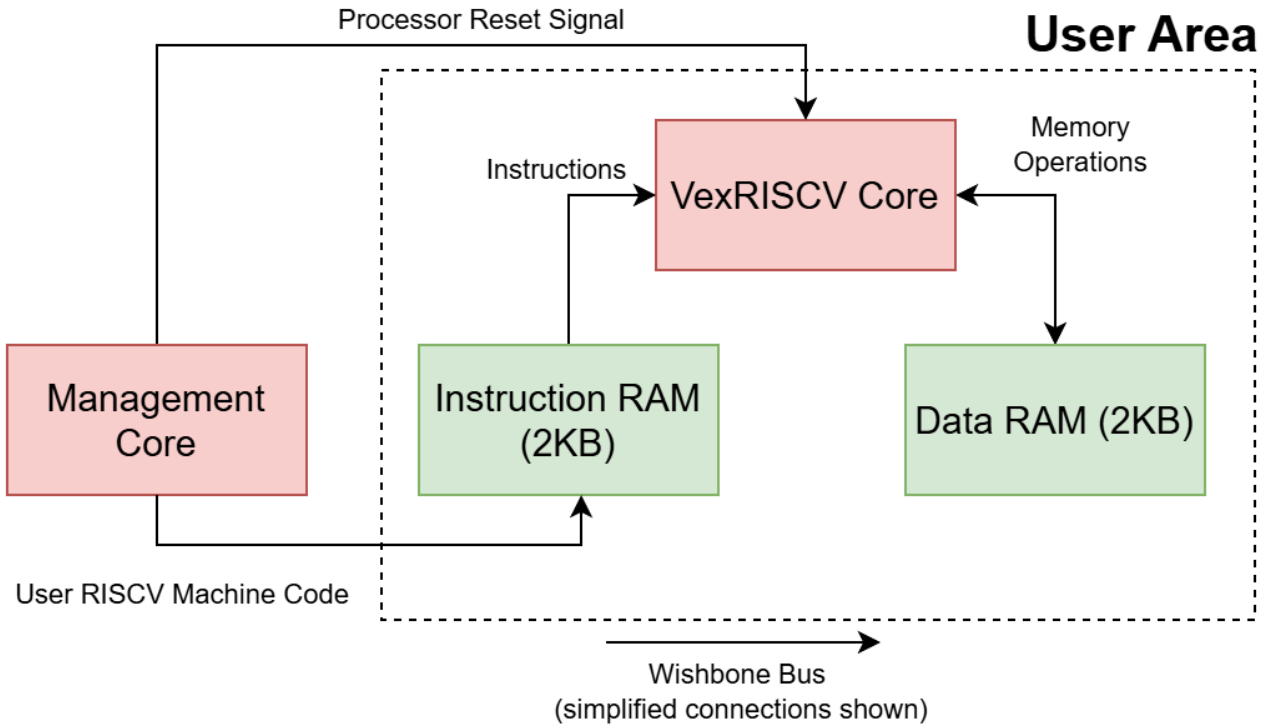
Digital Design – Wishbone Crossbar

- Need a way to control access to memory while also maintaining high performance
- Wishbone crossbar allows parallel access to different modules
- Wishbone crossbar prevents simultaneous access to same module
- Prototyped in first semester as proof of concept
- A script was written to make the crossbar generic, allowing easy expansion to accommodate new modules
- DD 70, 101



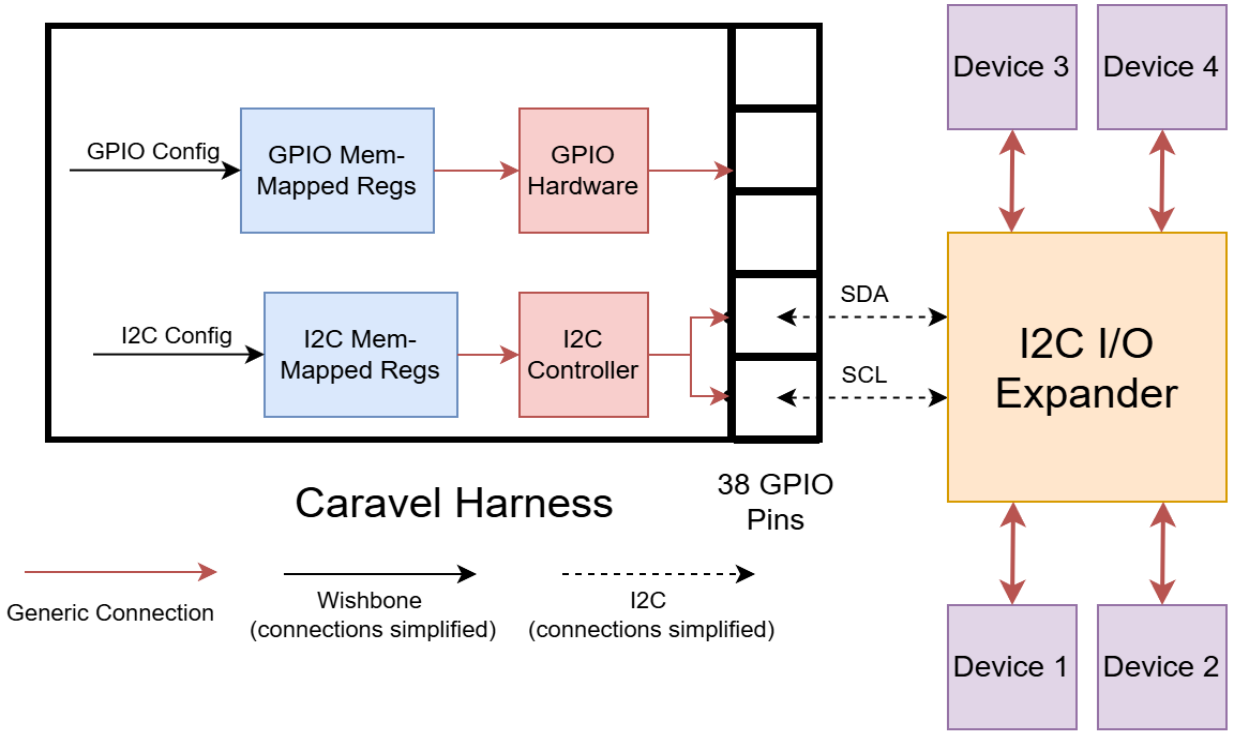
Digital Design – RISCV Core and RAM

- A RISCV core in the user area will run user programs
  - Generated using VexRISCV, which is open source and Wishbone compatible
- Instruction and data RAMs must be available to the user area RISCV core
  - Used existing Efabless DFFRAM macros and wrote a Wishbone slave interface for them
    - 2KB for instruction RAM
    - 2KB for data RAM
- DD 72, 92



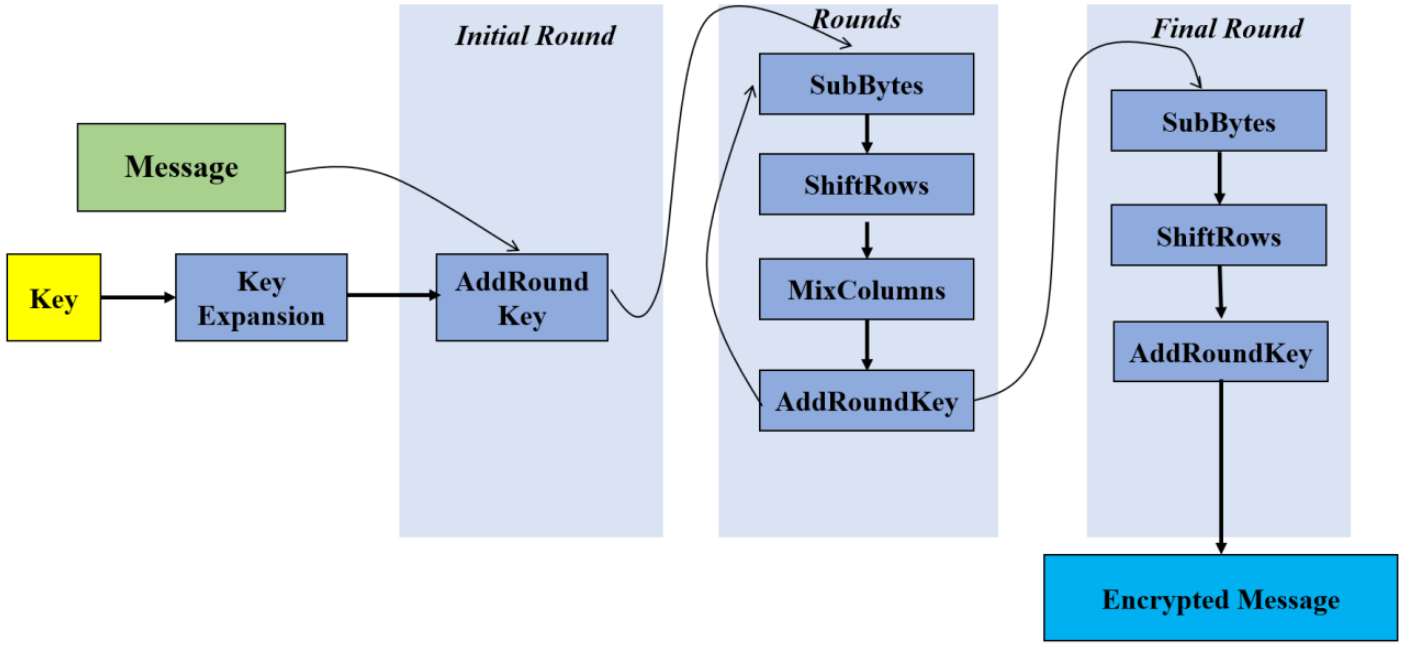
Digital Design - Peripherals

- General purpose input/output (GPIO)
  - Provided by Caravel harness
- Inter-integrated circuit (I2C)
  - Configured via memory-mapped registers
  - Uses GPIO with pullup resistors for SDA and SCL
    - I2C controller implemented in hardware
- DD 70, 92



Digital Design – AES Accelerator

- Evaluated potential security threats in radio microcontrollers (DD 133)
- Encryption is a crucial feature in wireless communication.
- AES was chosen due to its efficiency and being part of ZigBee.
- We chose to implement an open-source option from the Efabless marketplace. (DD 105)



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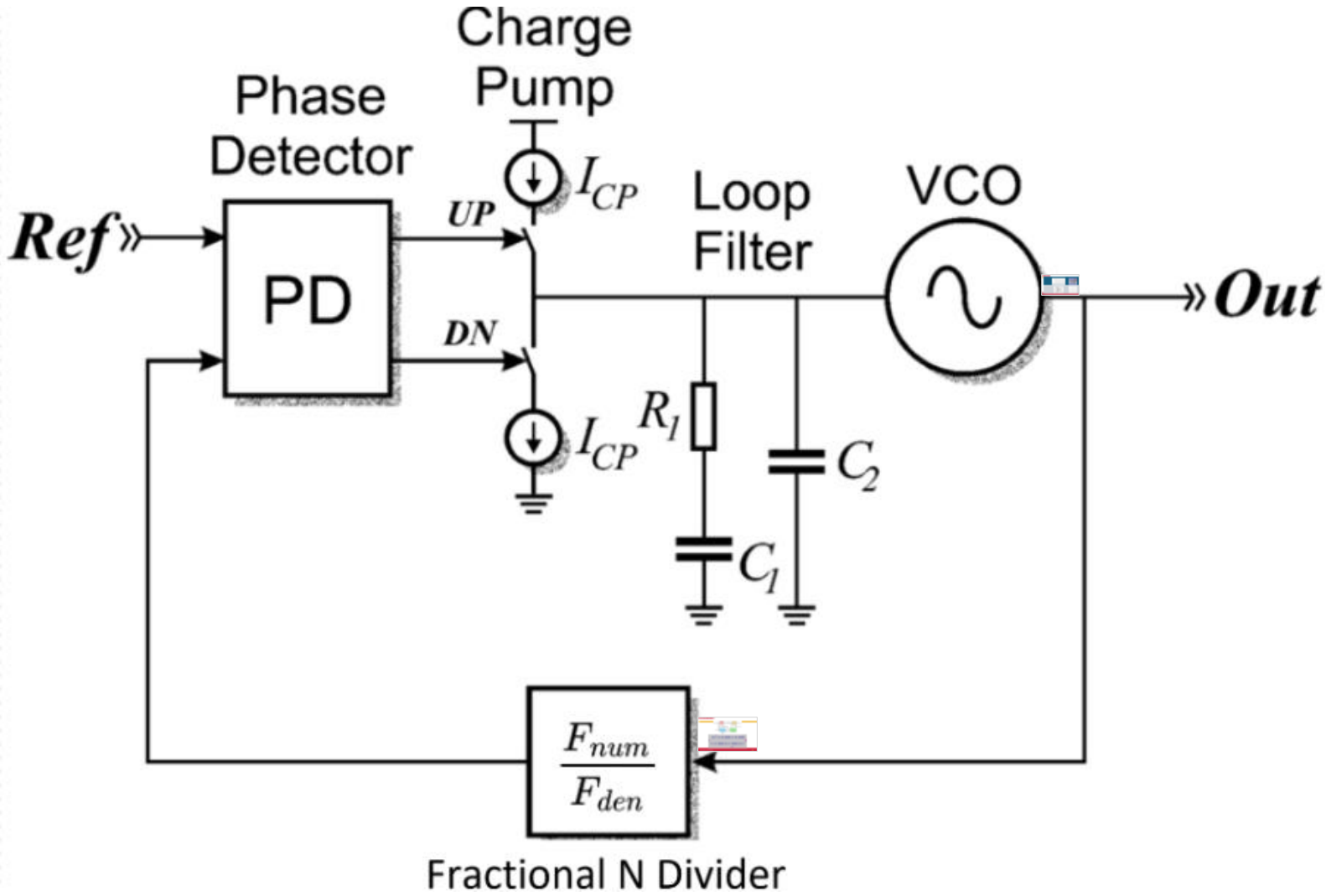
Analog Design – Frequency Synthesizer



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Unexpected Risk – Efabless Shutdown

- We found out in late March that Efabless has shutdown
- We will not be able to fabricate our chip
- We still can implement our project and run tests
- Layouts can also still be generated so if Efabless comes back, we will be set to send our design off for fabrication
- DD 31

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Shutdown Notice

Due to funding challenges, Efabless has shut down operations until further notice.
We regret any inconvenience and will provide updates as available.

[16]

Testing Plan DD 65

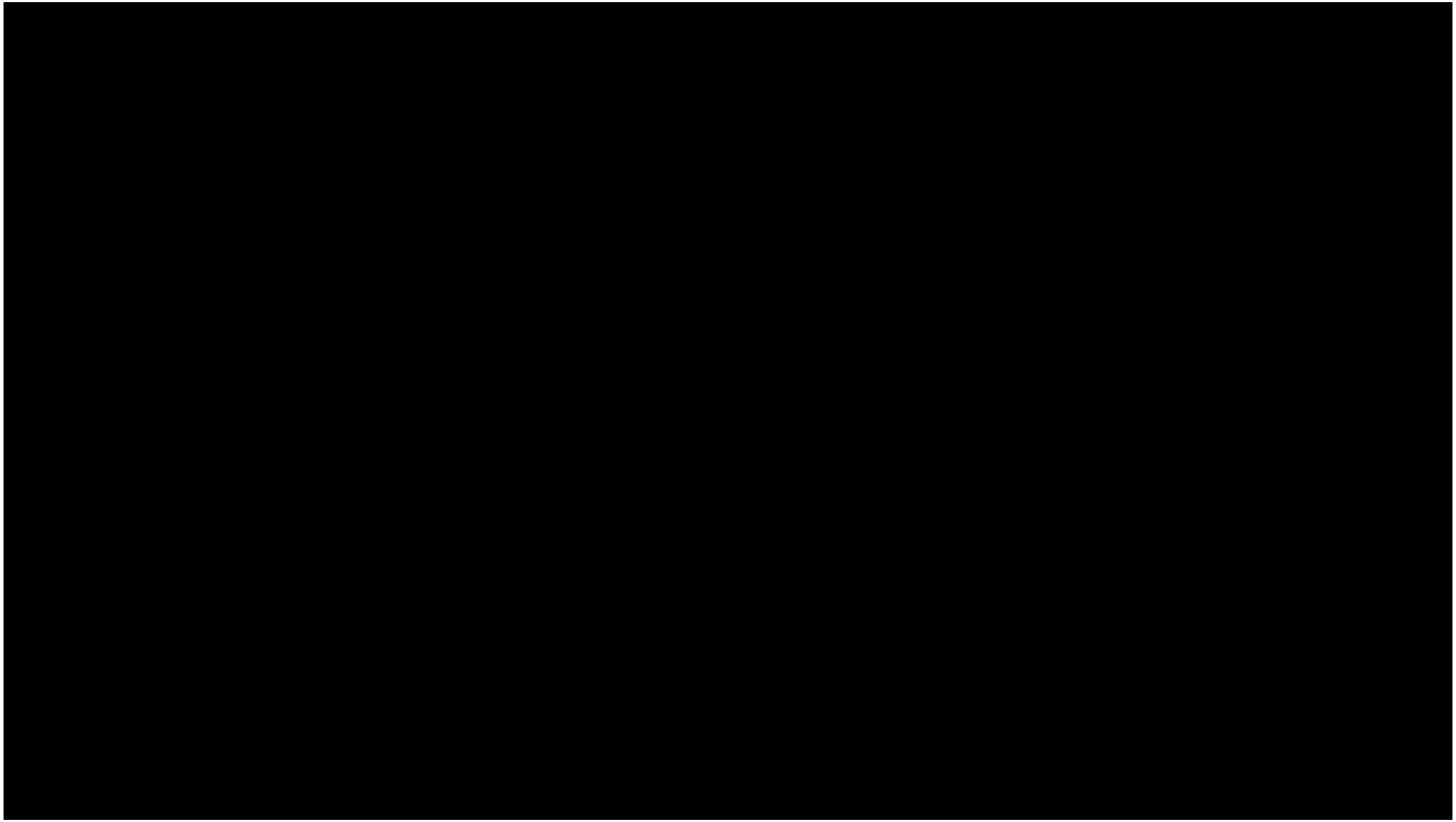
Digital	Analog	Security
RTL Verilog component simulation	Prelayout component simulation	Round Keys & S-Box
RTL full system simulation	Prelayout full system simulation	Message Authentication Codes
Hardware verification on FPGA	Layout components	CCM* Cipher Mode
	Postlayout simulation with extracted netlist	Encryption & Decryption

Digital Results

Wishbone Crossbar	Second RISCV Core	DFF RAM	I2C	AES
• Parallel access verified • Arbitration verified • Address mapping verified	• Reset verified • Program execution verified	• Reads and writes verified • Half word and byte reads and writes verified • Confirmed to synthesize and function on FPGA	• Addressing verified • Reads and writes verified • Multi-byte reads and writes verified	• Message Authentication Verified • Encryption & Decryption Verified

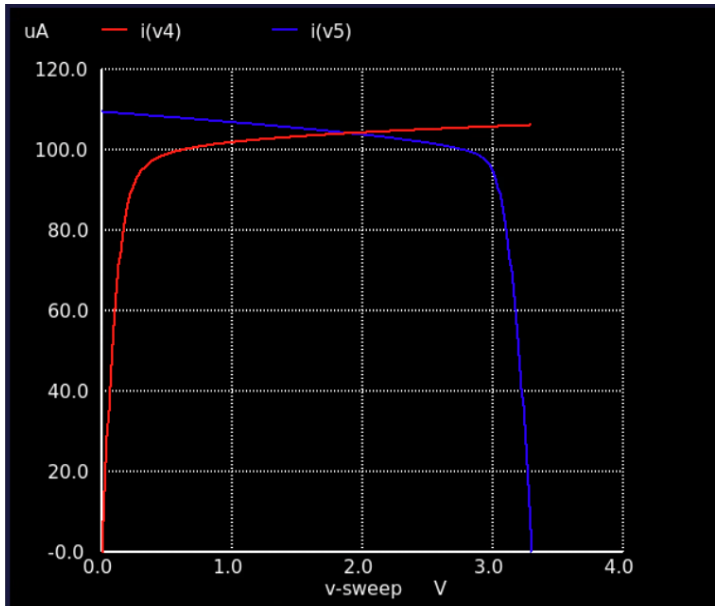
DD 78-86

Digital Demo Video

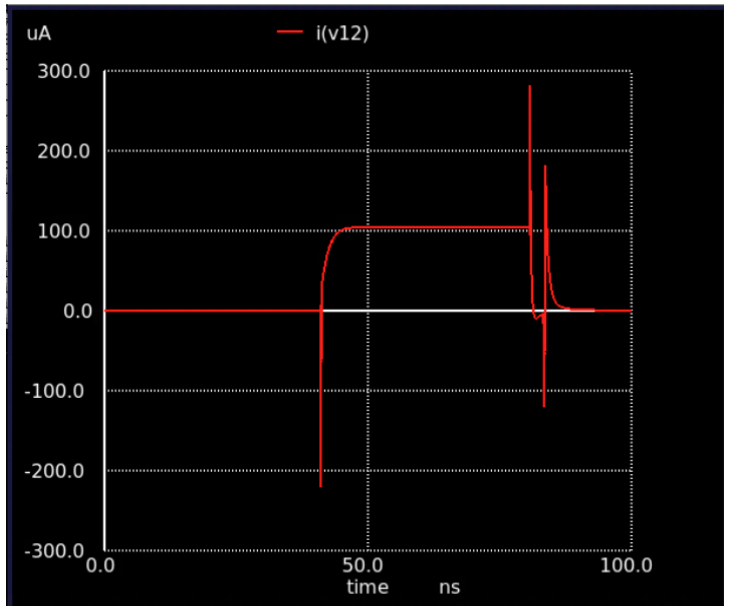


Analog Results DD 84

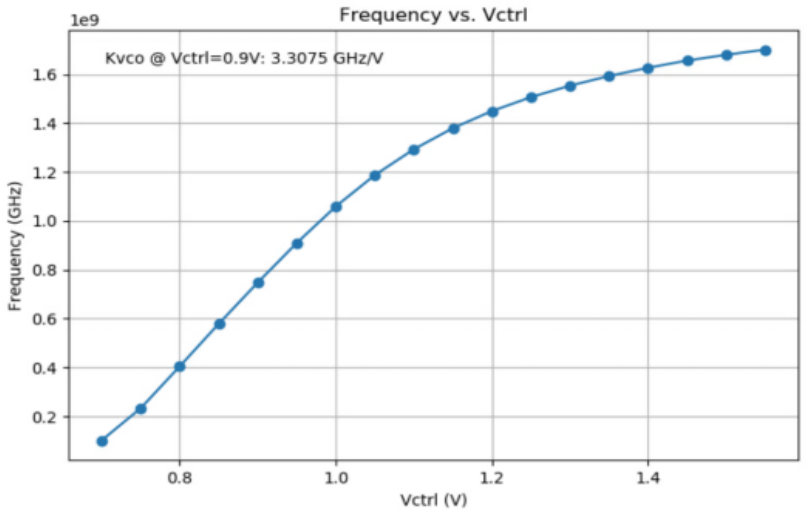
Charge Pump

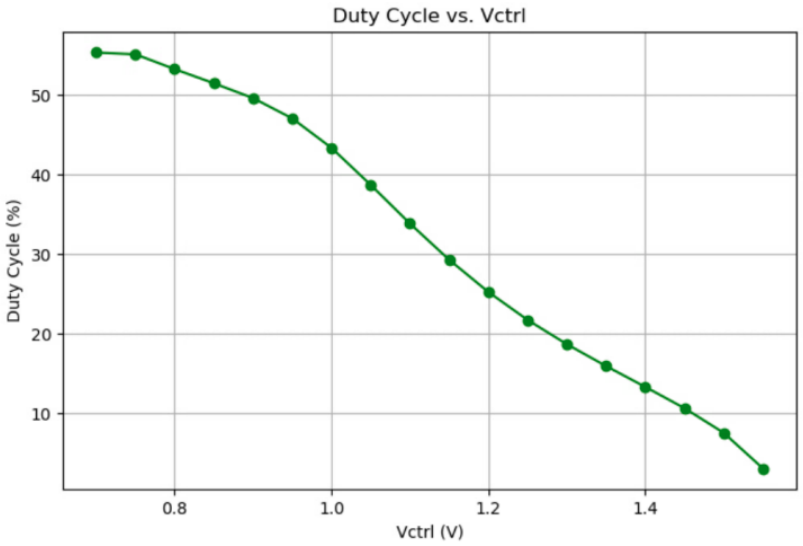


PFD and Charge Pump

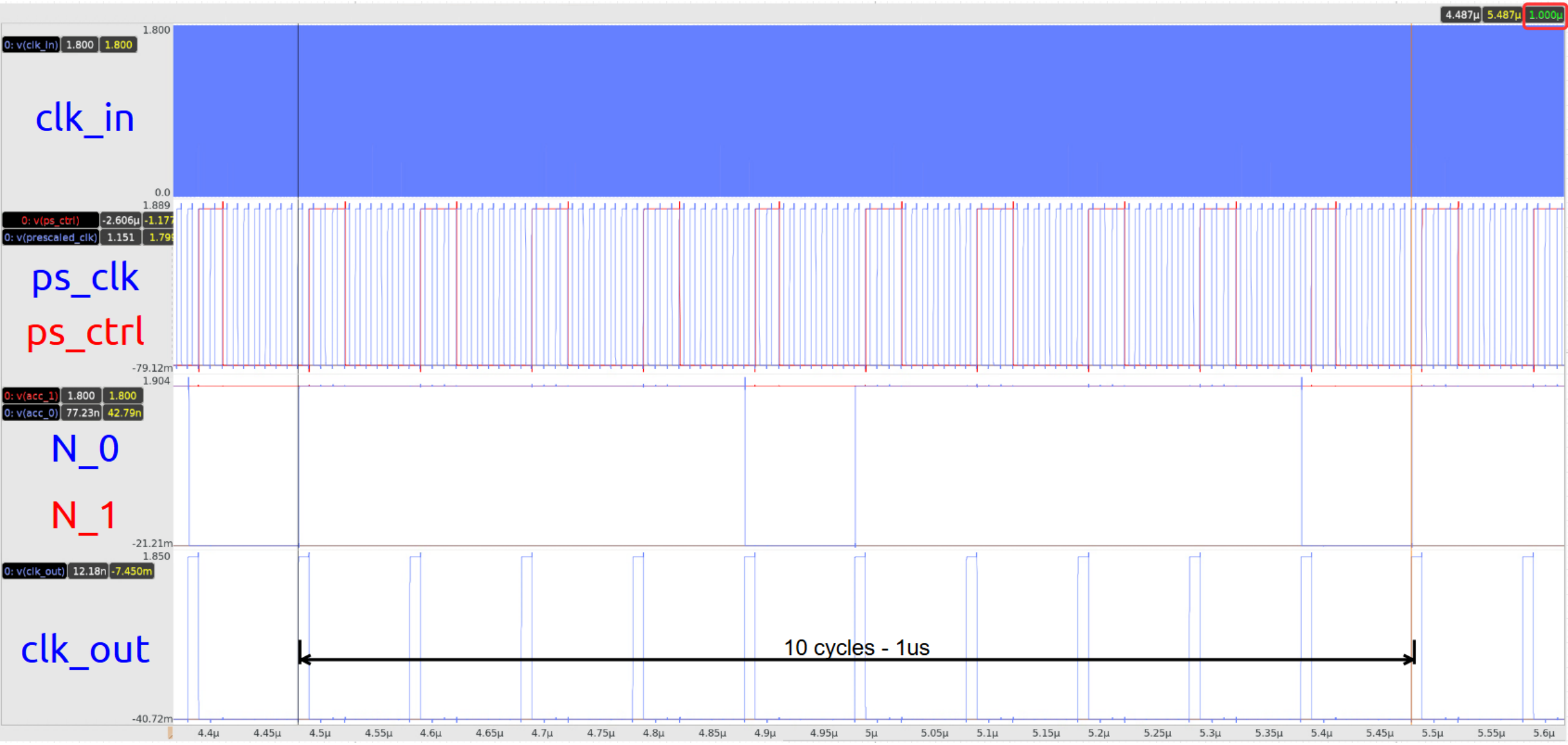


VCO



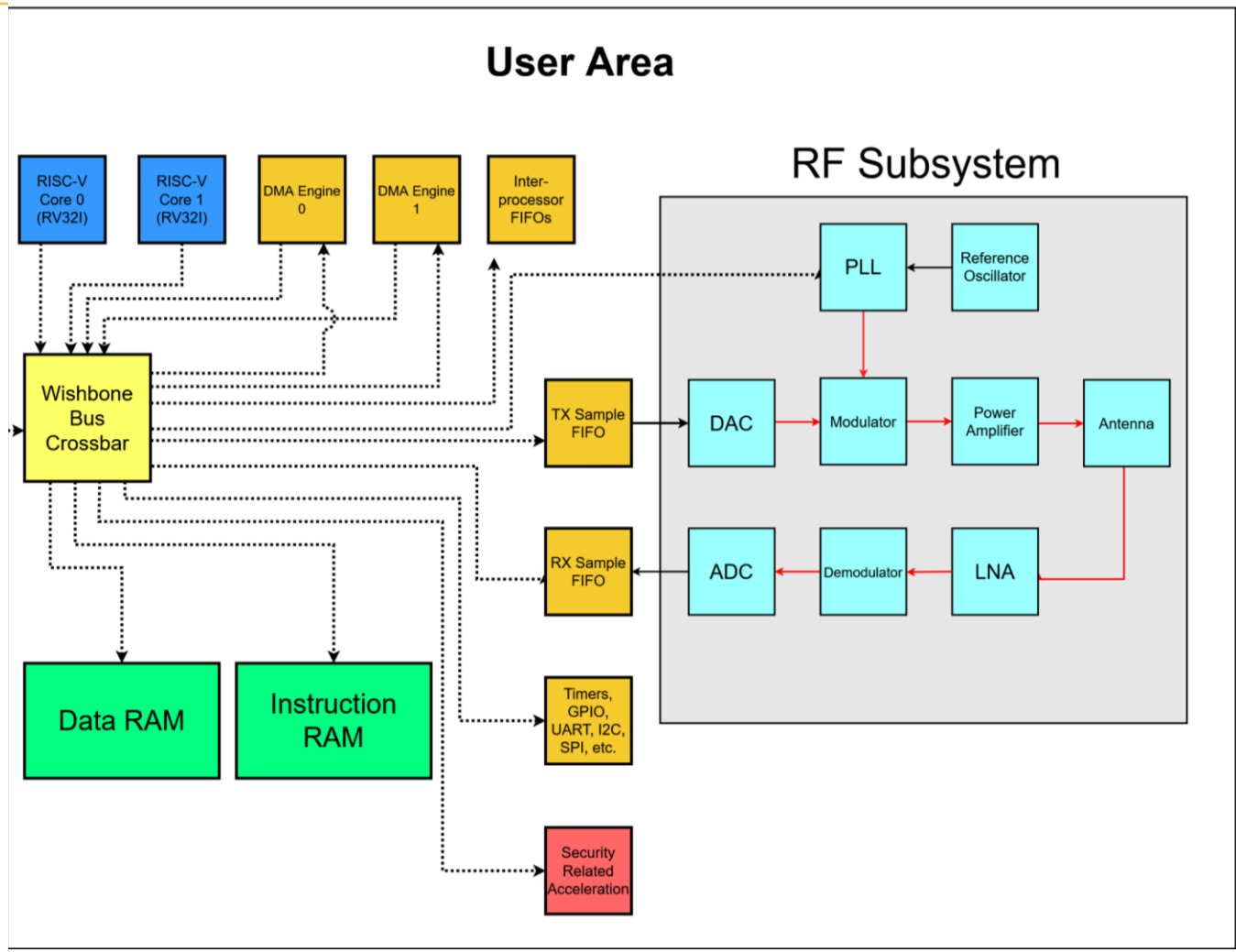


Analog Results – Fractional Divider DD 87



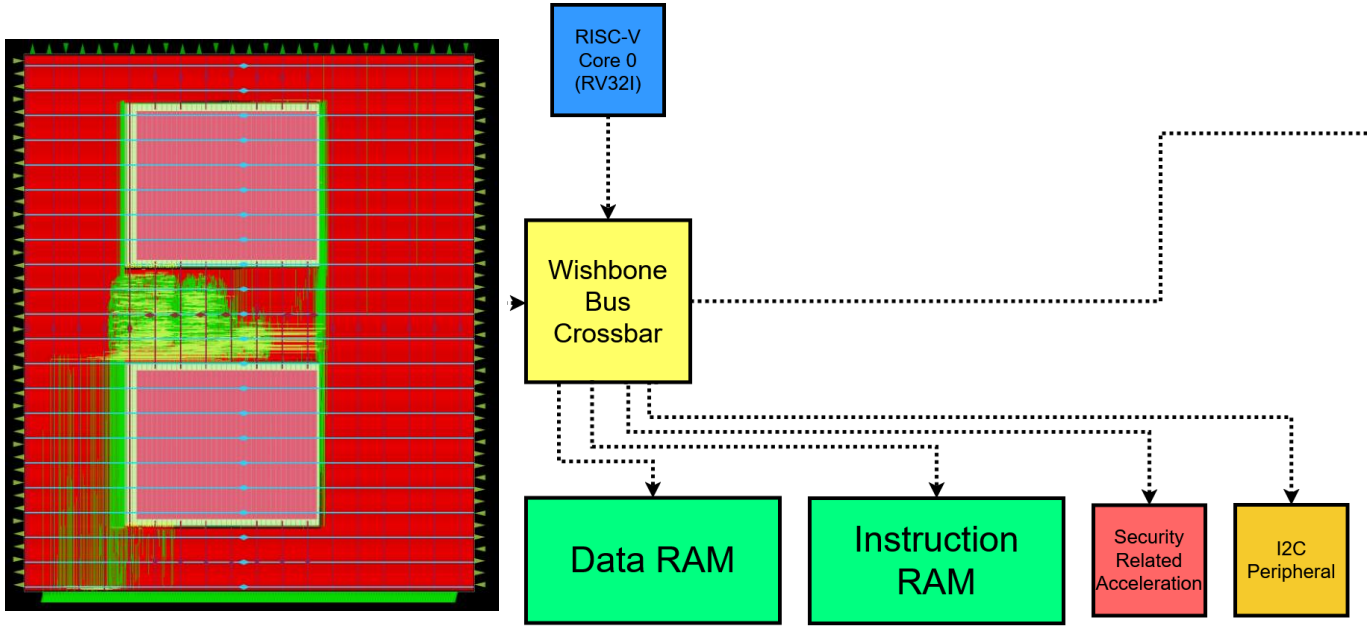
Future Work

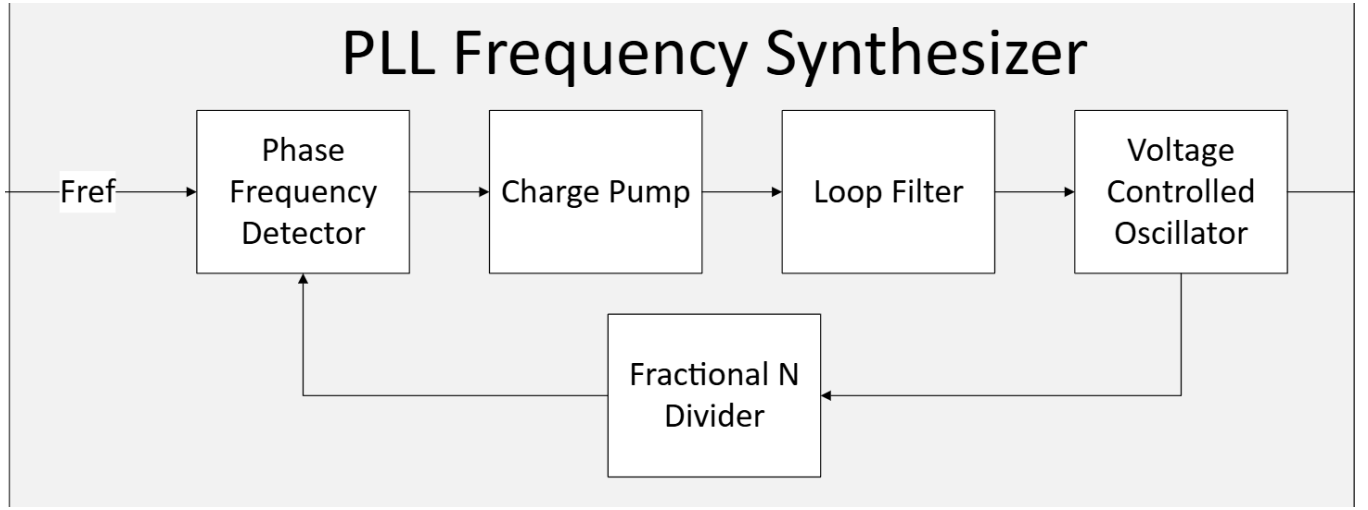
- Continue to expand on the design with the plan of developing it into diagram shown in the detailed design that includes a more well outlined digital and RF subsystem.
- Add and continue to refine documentation as project develops.
- Expand software libraries as digital and analog components are added.
- Integration of both digital and analog subsystems.
- Fabrication of the MCU



Conclusions – What We Have Accomplished

- Substantial progress in creating the components for a fully functioning open-source radio microcontroller
- Second RISCV core
- DFF RAM
- Wishbone Bus Crossbar
- I2C
- AES 128-bit encryption
- Divider
- PFD
- Charge-pump
- VCO





Questions?

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Image References

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[17] "Efabless Logo" Accessed: 5/6/2025. [Online]. Available: https://store.efabless.com/cdn/shop/files/logo_large_4fb22d13-6eef-4eac-9cd6-c7cd23939317.png?height=628&pad_color=ffffff&v=1702973184&width=1200

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Extra Slides

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Quantitative Technical Requirements

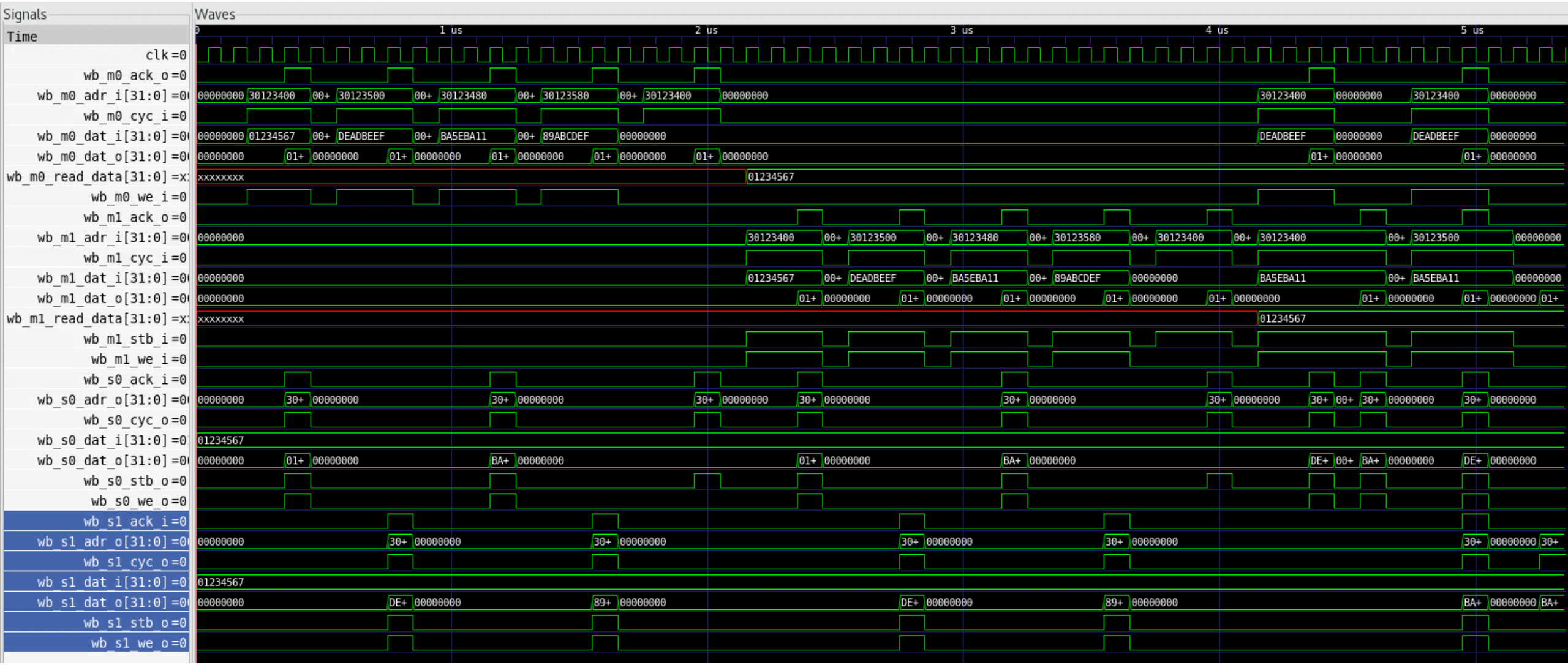
- The radio signal's phase noise will be below -41dBm/100Hz at a 32MHz offset per IEEE standard 802.15.4
- The radio signal's spurious emissions will be below -20dBc per IEEE standard 802.15.4
- The design shall contain 4 KiB of RAM accessible to the user
  - 2 KiB for data
  - 2 KiB for instructions for second RISCV core
- All Wishbone masters and slaves will use a 10 MHz reference clock which will be shared with the management SoC
- Die space limited to 2.92 mm x 3.52 mm

Security Analysis

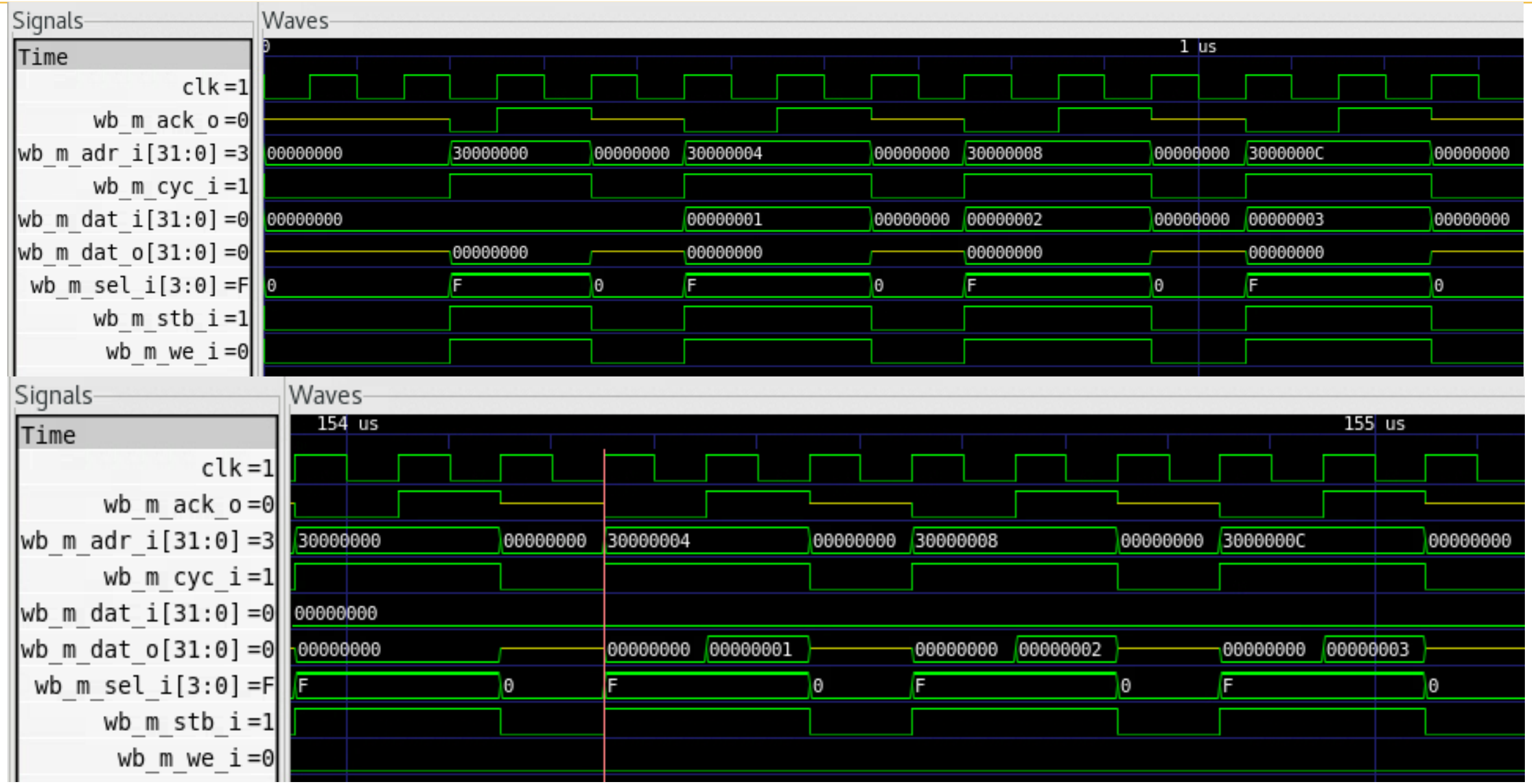
Vulnerabilities	Countermeasures
• Control flow manipulation • Fault attacks • Side-channel attacks • Sniffing data • Replay attacks • Repairing attacks	• Encryption • Authentication • Code obfuscation

Due to the scope of the project not every possible vulnerability could be addressed. Encryption made the most sense to be the first security measure implemented due to over the air communications being incredibly easy to intercept. As the project continues to develop with future groups, we hope that more of these security measures will be implemented.

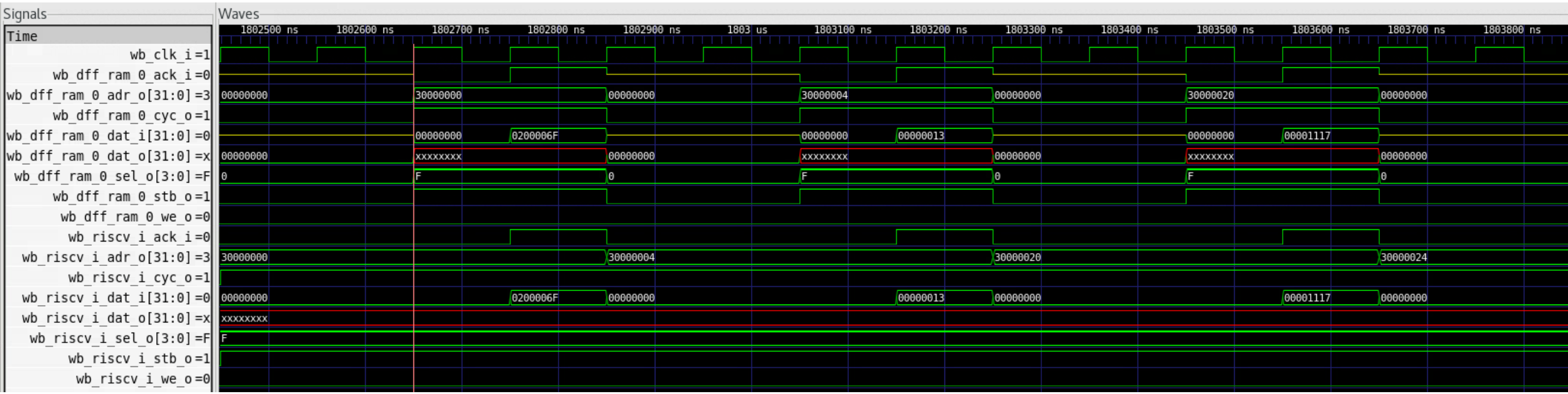
Crossbar Simulation Waveform



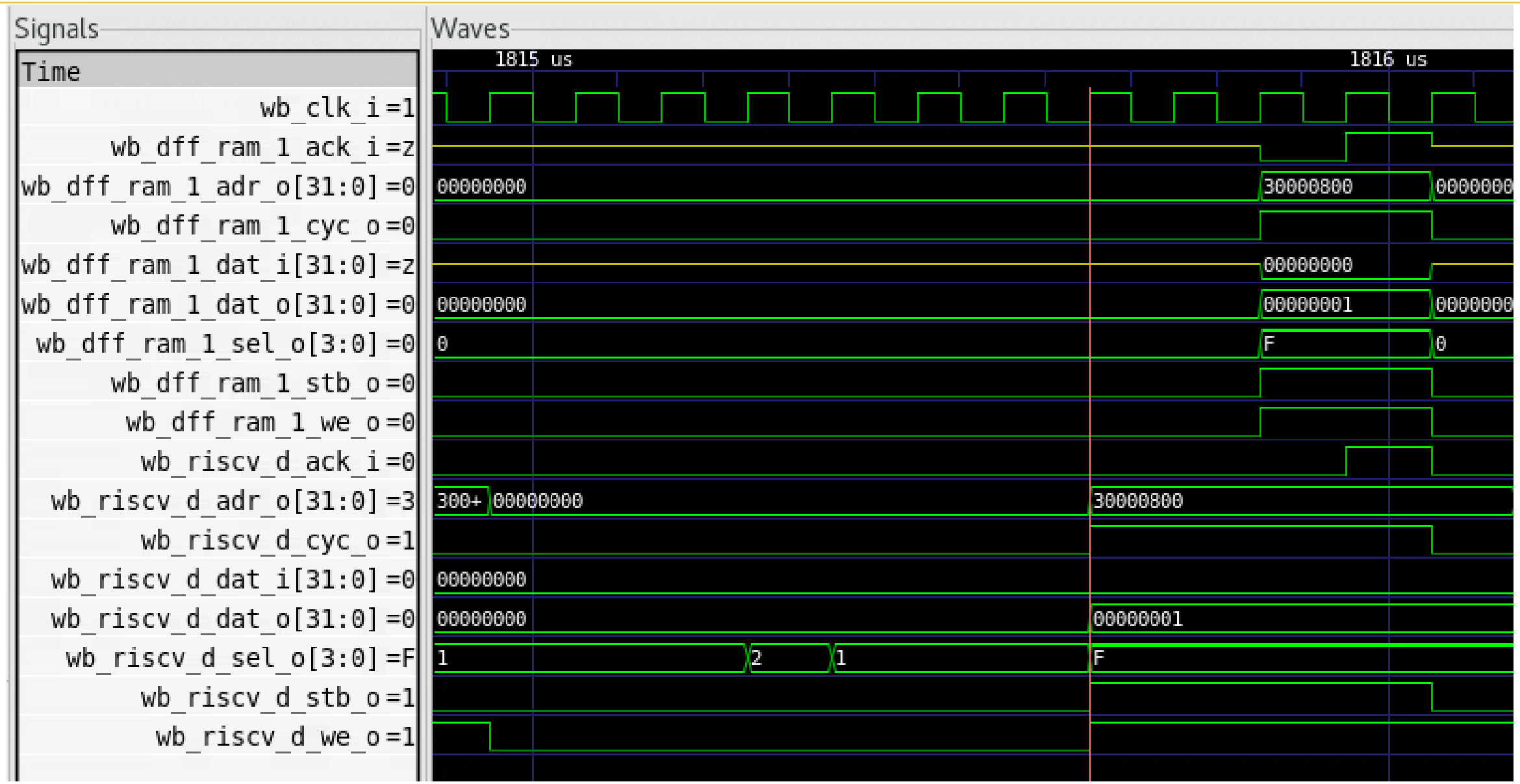
DFF RAM Waveforms



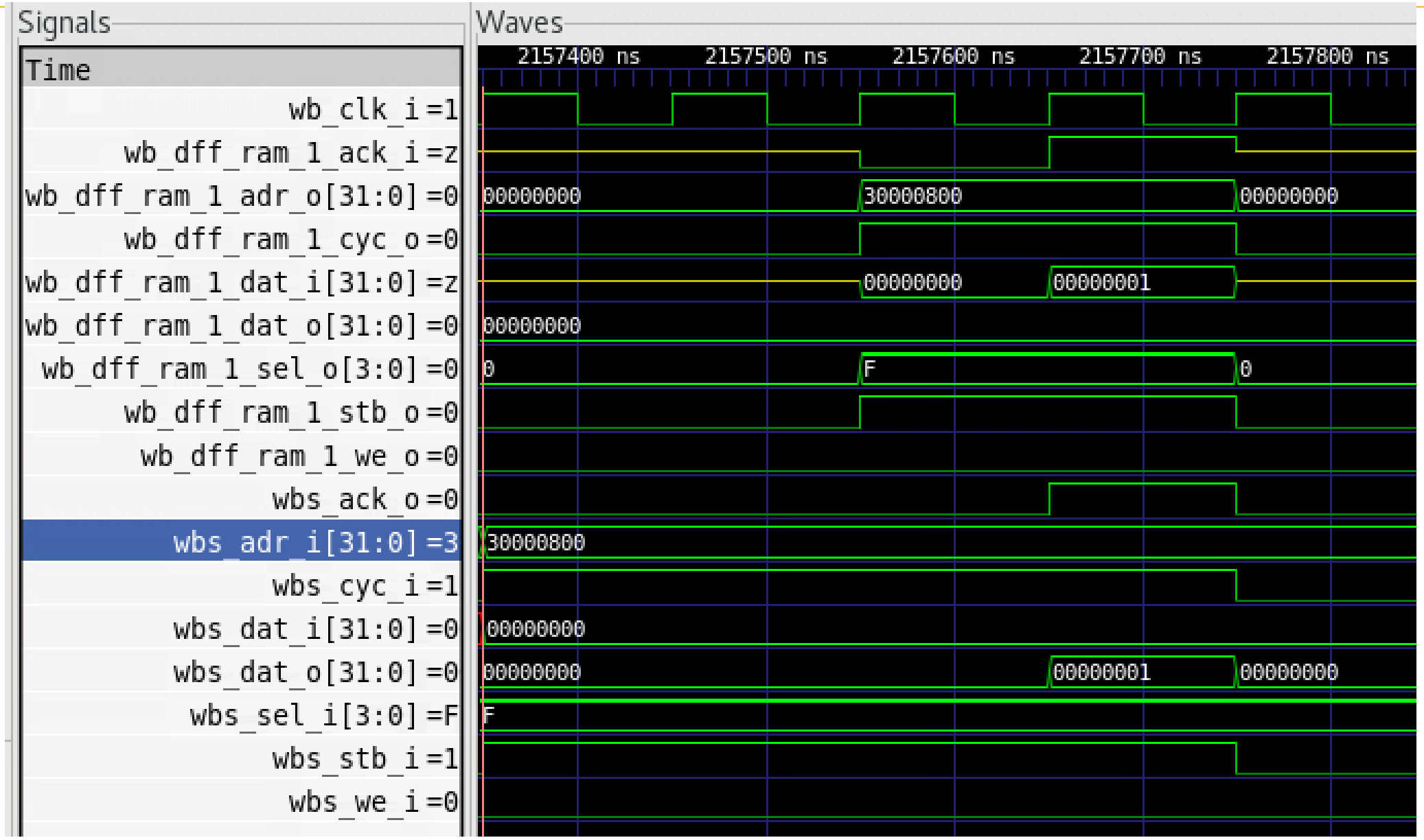
RISC-V Instruction Fetch



RISC-V Data Write

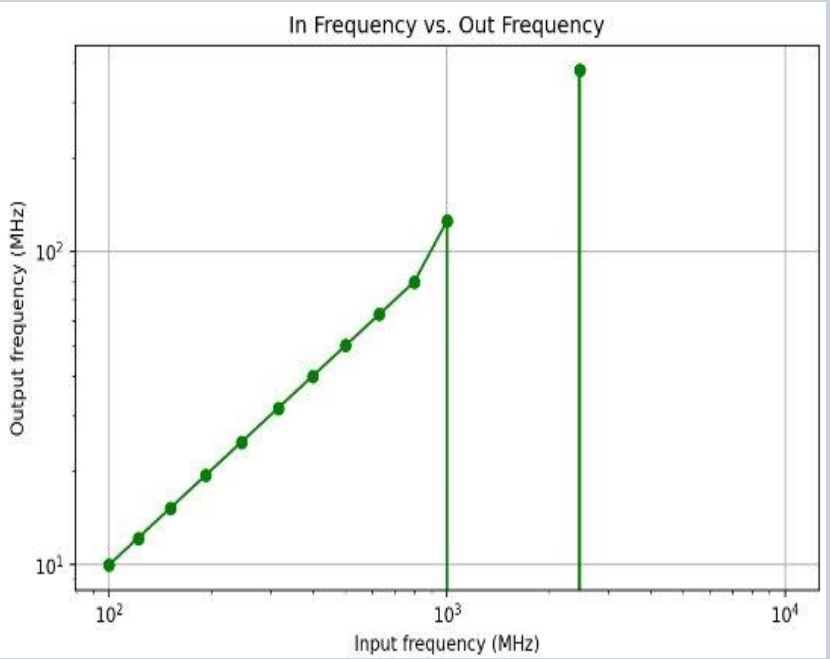


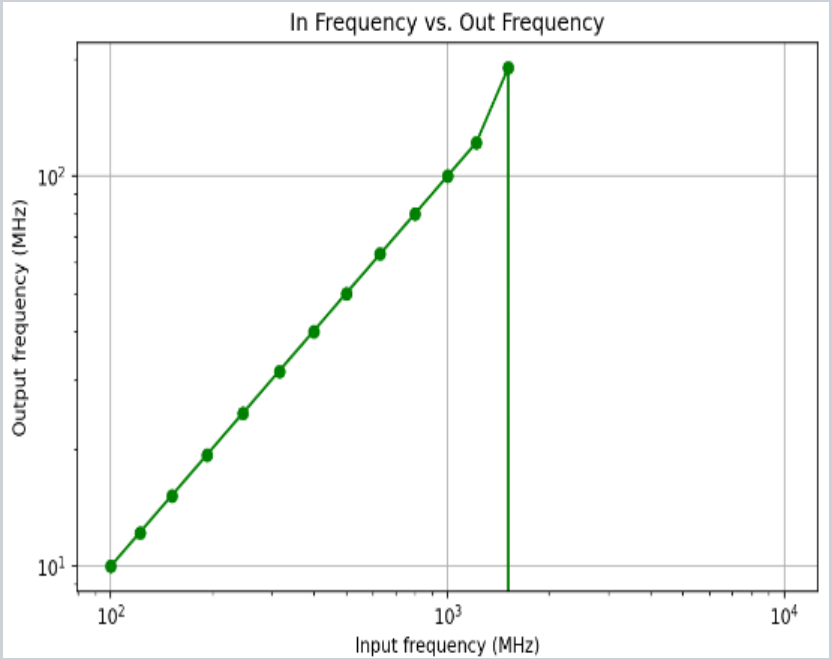
RISC-V Data Read

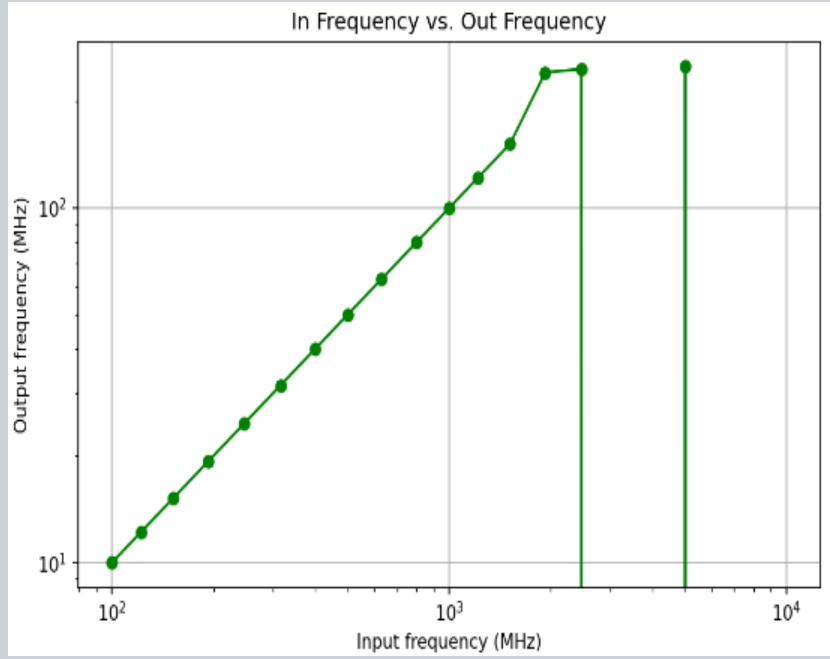


Divider Sweep Results

Corners - ss	Corners - tt	Corners - ff
Breakdown past 800MHz	Breakdown past 1.2GHz	Breakdown past 1.5GHZ



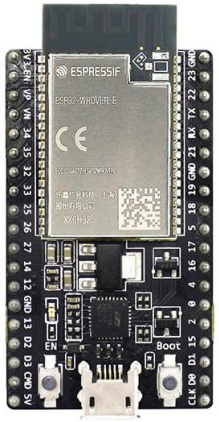




Problem Statement

- Existing **radio** microcontroller units (MCUs) have closed source designs
- Difficult for ISU students, ChipForge (ASIC design ISU club) members, and radio hobbyists to learn about how **radio** MCUs work
- Need an open-source MCU design that can be fabricated (silicon proven)

Closed Source Radio MCUs



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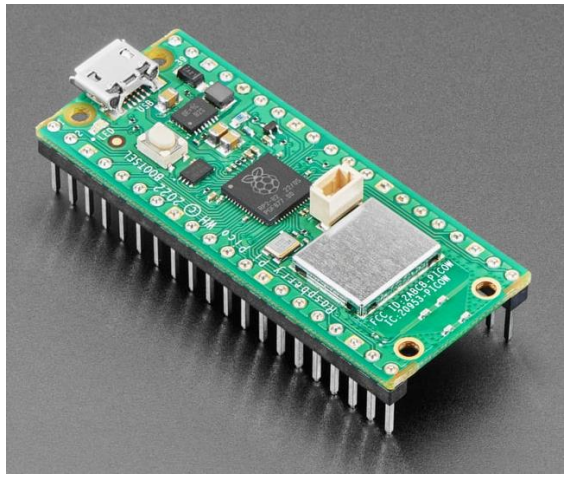

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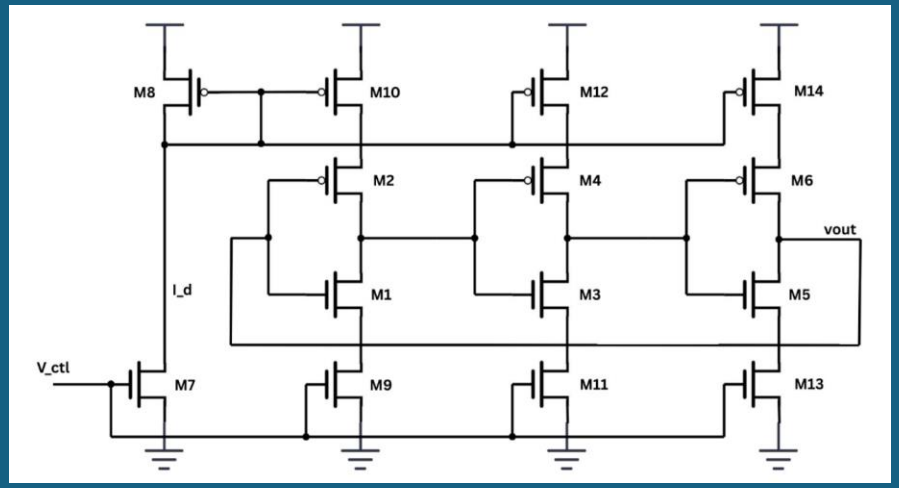
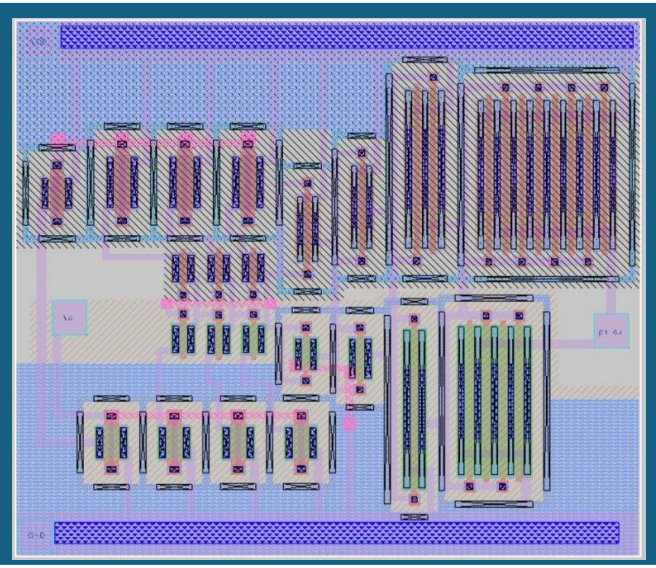
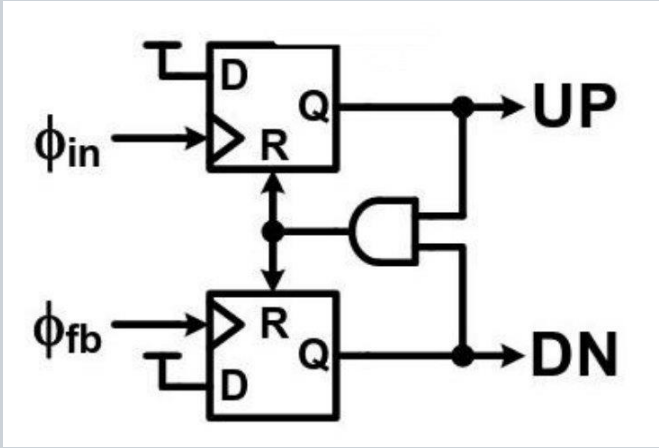
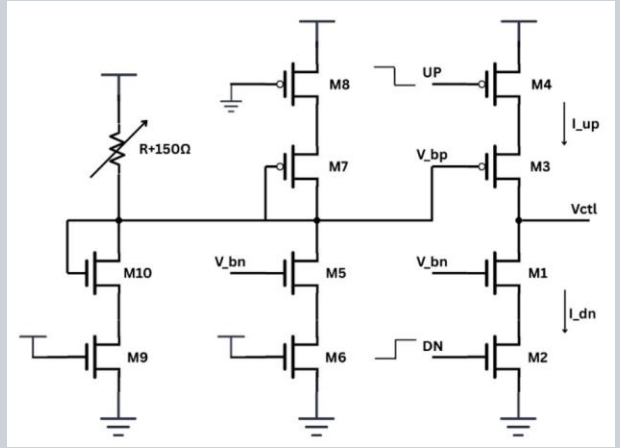
Security Testing Results

VCO, PFD, CP


M8
M10
M12
M14
M2
M4
M6
vout
I_d
M1
M3
M5
V_ctl
M7
M9
M11
M13




D
Q
R
UP
ϕin
ϕfb
R
Q
D
DN


M8
UP
M4
I_up
R+150Ω
M7
V_bp
M3
Vctl
M10
V_bn
M5
V_bn
M1
I_dn
M9
M6
DN
M2

Fractional Divider